Doc Code: AP.PRE.REQ

PTO/SB/33 (07-09)
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PRE-APPEAL BRIEF REQUEST FOR REVIEW

Docket Number (Optional)
100.152US01

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Signature_____

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Application Number	Filed
10/087,610	3/1/2002

First Named Inventor
Nichols

Art Unit	Examiner
2634	Linda Wong

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a notice of appeal.

The review is requested for the reason(s) stated on the attached sheet(s).
Note: No more than five (5) pages may be provided.

I am the

☐ applicant/inventor.

☐ assignee of record of the entire interest.
See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed.
(Form PTO/SB/96)

☒ attorney or agent of record.
Registration number 43868

☐ attorney or agent acting under 37 CFR 1.34.
Registration number if acting under 37 CFR 1.34. _____

/Jon M. Powers/
Signature

Jon M. Powers
Typed or printed name

952-465-0760
Telephone number

2010-09-10
Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

☐ *Total of _____ forms are submitted.

This collection of information is required by 35 U.S.C. 132. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11, 1.14 and 41.6. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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Applicant(s)	Nichols	PRE-APPEAL BRIEF CONFERENCE REQUEST ARGUMENTS
Serial No.	10/087,610	
Filing Date	3/1/2002	
Group Art Unit	2634	
Examiner Name	Linda Wong	
Confirmation No.	7953	
Attorney Docket No.	100.152US01	
Title: DIGITAL PLL WITH CONDITIONAL HOLDOVER		

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Applicant requests review of the Office Action mailed on June 10, 2010 in the above-identified application. No amendments are being filed with this request. This request is being filed with a Notice of Appeal reinstating the appeal previously filed in the present application. The review is requested for the reasons stated below.

REMARKS

Claim 1 of the present application recites, in relevant part, "wherein the processor is further coupled to receive a status message from a ***source*** of the ***reference*** clock signal indicative of a quality level of the ***reference*** clock signal".

The Examiner conceded that the primary reference, Johnson, fails to disclose "wherein the processor is further coupled to receive a status message from a source of the reference clock signal indicative of a quality level of the reference clock signal". See paragraph vi on page 4 of the Office Action.

The Examiner further took the position that "Zampetti et. al. discloses a stratum clock state machine or processor (Fig. 1, label 105) [that] receives status messages (labels 107 and 108 [*sic* – 109]) from a source (labels 102 and 105) of the reference clock signal (label clock a, clock b) that indicates the status of the reference clock signal." See paragraph v on pages 4-5 of the Office Action.

Applicant respectfully traverses these rejections.

First, the Office Action fails to set forth a *prima facie* showing of obviousness since the Examiner has not explained how Zampetti teaches "***a status message*** from a source of the reference clock signal ***indicative of a quality level*** of the reference clock signal" as recited in claim 1 of the present application. In this regard, the Examiner only alleges that the alleged "status messages" indicate "the status of the reference clock signal". No explanation is provided regarding how this teaches the actual claim language of "indicative of a quality level of the reference clock signal".

Second, the Examiner has made *clear factual errors* in its characterization of what Zampetti teaches.

The status-A and status-B lines 107 and 109 of Zampetti do NOT refer to clock-A 106 and clock-B 108 output by the input clock DPLL A 102 and input clock DPLL B 103 of Zampetti, respectively. Instead, they clearly refer to the *inputs* of the DPLLs 102 and 103 – that is, the 8 kHz clocks 100 and 102. See, e.g., Zampetti, column 6, lines 39-45 ("Referring to FIG. 1, ***the digital input phase-locked loop A 102 and the digital input phase-locked loop B 103*** can include all typical digital phase-locked loop component blocks, and also feature a state monitoring mechanism to determine ***what types of transients are occurring at the input. These states are fed into the stratum clock state machine 105 for processing***.").

However, the alleged status information communicated on the status-A and status-B lines 107 and 109 is not received from ***a source*** of the 8 kHz clocks 100 and 102 received on the inputs of the DPLLs 102 and 103. Instead, the alleged status information communicated on the status-A and status-B lines 107 and 109 is generated locally in the DPLLs 102 and 103. See, e.g., Zampetti, column 6, lines 39-45 ("Referring to FIG. 1, ***the digital input phase-locked loop A 102 and the digital input phase-locked loop B 103*** can include all typical digital phase-locked loop component blocks, and ***also feature a state monitoring mechanism to determine what types of transients are occurring at the input.*** These states are fed into the stratum clock state machine 105 for processing.").

In other words, in this regard, Zampetti merely teaches locally determining when there has been a loss of an input clock signal to one of the DPLLS 102 and 103. See, e.g., Zampetti, Column 6, lines 29-33 ("If there is a ***loss of input***, the stratum clock state machine

105 can command the main clock PLL 110 to use the historical controller, preventing ***transience*** from affecting the main clock PLL 110 at the moment it goes on the holdover."). ***This is what Johnson already does – locally determine when there has been a loss of an input clock and, therefore, Zampetti does not cure the admitted defects with the teachings of Johnson.***

The Examiner does not allege that any of the other cited references teach this language from claim 1.

Applicant respectfully submits that the arguments set forth above generally apply to all of the outstanding rejections. Applicant, however, does not concede any assertion made in the Office Action with respect to these claims and reserves the right to provide additional arguments directed to these claims if a further response is required.

If necessary, please charge any additional fees or credit overpayments to Deposit Account No. 502432.

If the Examiner has any questions or concerns regarding this application, please contact the undersigned at 952-465-0760.

Respectfully submitted,

Date: 2010-09-10	/Jon M. Powers/

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